(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
21 June 2001 (21.06.2001)

PCT

(10) International Publication Number
WO 01/45263 A1

(51) International Patent Classification⁷: H03L 7/081, 7/18, H03K 5/00, 23/68

(21) International Application Number: PCT/US00/33908

(22) International Filing Date: 14 December 2000 (14.12.2000)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/170,621 14 December 1999 (14.12.1999) US

(71) Applicant *(for all designated States except US)*: **BROADCOM CORPORATION** [US/US]; 16215 Alton Parkway, Irvine, CA 92618-3616 (US).

(72) Inventors; and
(75) Inventors/Applicants *(for US only)*: **FALLAHI, Siavash** [IR/US]; 16215 Alton Parkway, Irvine, CA 92618-3616 (US). **WAKAYAMA, Myles** [US/US]; 16215 Alton Parkway, Irvine, CA 92618-3616 (US). **VORENKAMP, Pieter** [NL/US]; 16215 Alton Parkway, Irvine, CA 92618-3616 (US).

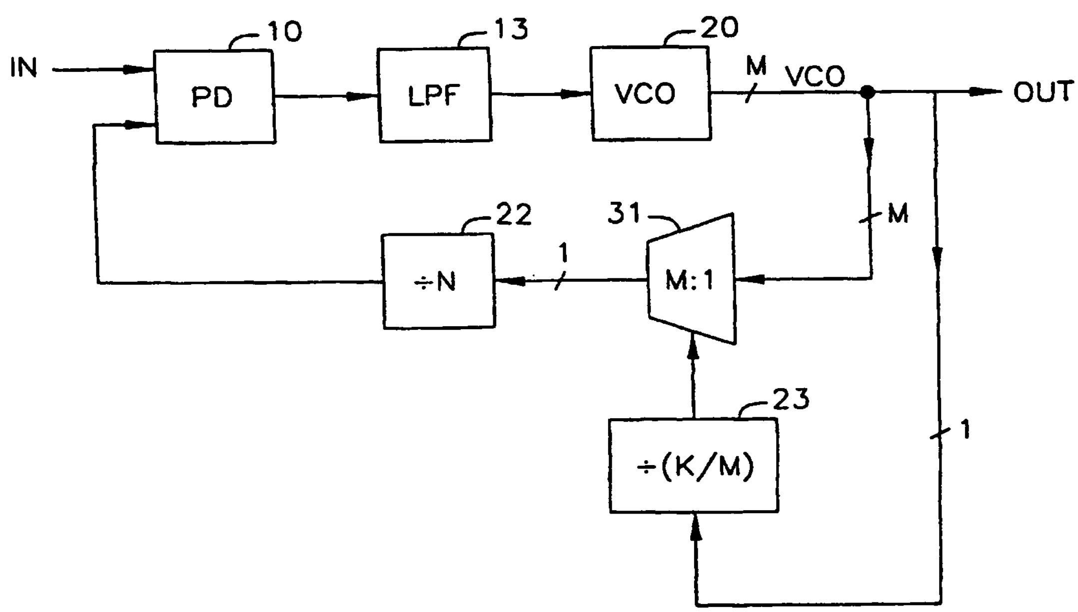
(74) Agent: **TABANDEH, Raymond, R.**; Christie, Parker & Hale, LLP, P.O. Box 7068, Pasadena, CA 91109-7068 (US).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

*[Continued on next page]*

(54) Title: FREQUENCY DIVISION/MULTIPLICATION WITH JITTER MINIMIZATION




(57) Abstract: A method and system described for producing frequency multiplication/division by any non-integer output signal frequency relative to a reference signal frequency of a Phase-Lock-Loop (PLL), while simultaneously maintaining low jitter. In one embodiment, the invention increases the number of the available clock phases to M and then shifts the output clock phase by one, every K/M cycle. In one aspect of the present invention, this is accomplished by adding a multiplexer (MUX) to the output of the PLL to implement the phase shifting every K/M cycles. In another aspect, the MUX is placed in the feedback loop of the PLL. In one embodiment, a quantizer is used to drive the MUX.

WO 01/45263 A1

**Published:**

- *With international search report.*
- *Before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments.*

*For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.*

# FREQUENCY DIVISION/MULTIPLICATION WITH JITTER MINIMIZATION

## FIELD OF THE INVENTION

The present invention is directed to a system for and a method of dividing or multiplying a reference frequency signal by a non-integer number while minimizing the introduction of timing jitter to the resultant output frequency signal.

## BACKGROUND OF THE INVENTION

The past several years have witnessed a dramatic increase in the capabilities of high-speed, high-density, broadband data communication systems. Such systems may range anywhere from broadcast or cablecast HDTV systems, local area and wide area network (LAN, WAN) systems, fiber to the home (FTTH) applications and board-to-board interconnections in exchange systems and computers.

In any one of the foregoing applications, it should be noted that bidirectional data communication is in digital form and, accordingly, clock and data recovery circuitry is a key component of the efficient functioning of modern data communications systems. The ability to regenerate binary data is an inherent advantage of transmitting information digitally as opposed to transmitting such information in analog form. However, in order for the intelligence signal to be correctly reconstructed at the receiving end, the transmitted binary data must be regenerated with the fewest possible number of bit errors, requiring low noise and timing jitter (phase noise) at the clock generation source. In high speed data communication systems, low jitters are important for ensuring low error rates.

Clock signal generation is traditionally performed by a Phase-Lock-Loop (PLL) system such as that illustrated in FIG. 1. A PLL operates to compare the frequency and/or phase of an incoming serial datastream to a periodic reference clock signal generated by an oscillator circuit, and to adjust the operational frequency and phase characteristics of the oscillator until its output stream is "locked" in both frequency and phase to the data signal. Frequency division and/or frequency multiplication can be used to generate multiple clock phases from a PLL.

FIG. 1 shows a typical PLL circuit that is used to perform a frequency signal multiplication (or division) function. A reference signal ("IN") is applied to one input of the Phase/Frequency Detector 10 where the phase and frequency of a feedback clock from a divider circuit 19 is compared. The Phase/Frequency detector 10 circuit outputs signals 16 & 18 to the charge pump circuit 12 indicating whether the feedback clock from the divider circuit is lower or higher in frequency and ahead or behind in phase. The charge pump converts the signals from the Phase/Frequency detector typically into analog current signals that are filtered by the Filter 13. The filtered signal is then output to the Voltage Controlled Oscillator (VCO) 14 which produces an output signal which is typically the output of the PLL ("OUT"). The output signal of the VCO is input to the divider circuit 19, which divides the frequency of the output signal by an integer

"N" in this example. The output signal of the divider circuit is input to the phase detector circuit completing the PLL. In this case, the output signal of the PLL is limited to integer multiples of the reference signal.

Non-integer multiply functions for the overall PLL can be implemented by placing a divider circuit (e.g., divide by D) at the output of the PLL thereby, dividing the output signal by D. This results in FOUT = FIN x N/D, where N/D is a non-integer number. However, when N becomes a large number, The frequency of the VCO may become unpractically large. Non-integer multiply/divide functions can also be implemented by designing the divider circuit 19 of FIG. 1A to appropriately suppress predetermined clock cycles to its input signal at a specific rate defined by a number "K", thereby decreasing its effective divide ratio by K+1/K. FIG. 1B is an exemplary timing diagram for a conventional non-integer division. As shown, every K cycles, one cycle of the OUT signal is suppressed, resulting in K cycles in K+1 periods. Therefore, the frequency of the OUT signal, FOUT = Number of cycles / Time = K/ (K+1). T, where T is the period for VCO. Thus, FOUT = FVCO x K/(K+1), that is dividing FVco by K+1/K.

However, these technique adversely cause large changes in the period of the output of the divider circuit introducing jitter to the output of the PLL. This jitter is as large as the period of the suppressed cycle, i.e., the period of the output signal of the PLL. This large jitter is very undesirable for most systems as described previously.

A non-monolithic implementation that can accomplish this function is commonly known as a VCXO. By applying a control voltage to a VCXO circuit its output signal frequency can be changed, or as commonly referred to, "pulled" to a desired frequency in the order of $\pm$1000ppm or less from its natural frequency. However, this implementation is very complex and costly.

Accordingly, prior art-type PLL circuits do not provide an integrated, low-cost, and simple frequency division/multiplication with low jitter. Accordingly, for high-speed PLLs, there is a demonstrated need for a frequency division/multiplication with low jitter which is designed and constructed such that jitters are substantially minimized.

## SUMMARY OF THE INVENTION

The present invention enables full flexibility to produce frequency multiplication/division by any non-integer output signal frequency (for example, (K+1)/K, or K/(K-1) ) relative to a reference signal frequency, while simultaneously maintaining low jitter performance.

In one embodiment, the invention shifts the phase of the OUT signal by one phase, every K/M cycle. In another embodiment, the invention increases the number of the available clock phases to M and then shifts the phase of the OUT signal by one phase, every K/M cycle. In one aspect of the present invention, this is accomplished by adding a multiplexer (MUX) to the output of the PLL to implement the phase shifting every K/M cycles. In another embodiment, the MUX is placed in the feedback loop of the PLL. In yet another embodiment, a quantizer is used to drive the MUX resulting in further minimization of noise.

In one aspect, the present invention describes an integrated low jitter frequency multiplication/division electronic circuit for multiplying/dividing frequency of a reference signal comprising: a PLL for generating M number of clock phases from the reference signal; and a signal shifter electrically coupled to the PLL for shifting the reference signal by one phase every K/M cycle, wherein (K+1)/K is a divisor number and K/(K-1) is a multiplier number.

In another aspect, the present invention describes a method for multiplying/dividing frequency of a reference signal comprising the steps of generating M number of clock phases; and shifting the reference signal by one phase every K/M cycle, wherein (K+1)/K is a divisor number and K/(K-1) is a multiplier number. In yet another aspect, the present invention describes a frequency division electronic circuit for dividing frequency of a reference signal by a non-integer number (K+1)/K, comprising: PLL for generating M number of clock phases from the reference signal; and a signal shifter electrically coupled to the PLL for shifting the reference signal by one phase every K/M cycle.

## DESCRIPTION OF THE DRAWINGS

These and other features, aspects, and advantages of the present invention will be more fully understood when considered with respect to the following detailed description, appended claims, and accompanying drawings, wherein:

FIG. 1A is a semi-schematic simplified block diagram of a PLL, in accordance with the prior art;

FIG. 1B is an exemplary timing diagram for a conventional non-integer division;

FIG. 2 is a semi-schematic simplified circuit diagram of a modified PLL in accordance to one embodiment of the present invention;

FIG. 3A is a series of timing diagrams illustrating the timing of the output signal in FIG. 2 for a frequency division in accordance to one embodiment of the present invention;

FIG. 3B is a series of timing diagrams illustrating the timing of the output signal in FIG. 2 for a frequency multiplication in accordance to one embodiment of the present invention;

FIG. 3C is a noise spectrum diagram in accordance to one embodiment of the present invention;

FIG. 3D is a series of timing diagrams illustrating the timing of the output signal in FIG. 2 for M = 4;

FIG. 4 is a semi-schematic simplified circuit diagram of a modified PLL in accordance to one embodiment of the present invention;

FIG. 5 is a semi-schematic simplified circuit diagram of a modified PLL in accordance to one embodiment of the present invention;

FIG. 6A is a simplified representation of a truncator used as a quantizer in accordance to one embodiment of the present invention;

FIG. 6B is a semi-schematic simplified circuit diagram of a modified PLL using the truncator of FIG. 6A;

FIG. 7A is a simplified representation of a random number generator used as a quantizer in accordance to one embodiment of the present invention;

FIG. 7B is a simplified plot of frequency vs. noise energy for the quantizer of FIG. 7A;

FIG. 7C is a semi-schematic simplified circuit diagram of a modified PLL using the random number generator of FIG. 7A;

FIG. 8A is a simplified representation of a quantizer using an integrator in accordance to one embodiment of the present invention;

FIG. 8B is a simplified plot of frequency vs. noise energy for the quantizer of FIG. 8A; and

FIG. 8C is a semi-schematic simplified circuit diagram of a modified PLL using the integrator of FIG. 8A.

## DETAILED DESCRIPTION OF THE INVENTION

The present invention minimizes jitters caused by frequency multiplication/division by a number of jitter reduction schemes and different combinations of those schemes. In one embodiment, to divide a frequency by a non-integer number such as (K+1)/K, the invention increases the number of the available clock phases to M and then shifts the output clock by one, every K/M cycle. Similarly, a frequency multiplication by a non-integer number such as K/(K-1) can be achieved by increasing the number of the available clock phases to M and then shifting the output clock in an opposite way by one, every K/M cycle. This technique of frequency division/multiplication decreases the jitter from T to T/M, resulting in a jitter improvement by a factor of M, because the discarded cycle is now 1/M of the original cycle. Exemplary timing diagrams for this technique of frequency division/multiplication are illustrated in FIG. 3A and 3B, respectively. The shifting function may be performed by a MUX or any other signal shifter.

FIG. 2 shows an exemplary implementation of this scheme. In this embodiment, VCO 20 is capable of producing M phases of clocks. MUX 21 is added to the output of the VCO to implement the phase shifting every K/M cycles. Counter 23 controls the select signals for MUX 21 and the feedback clock is divided by N in block 22. Note that, for simplicity reasons, the charge pump 12 of FIG. 1A is included in PD 10 of FIG. 2.

FIG. 3A is a simplified timing diagram for the circuit of FIG. 2 for performing frequency division. As shown by OUT signal, after K/M cycles, the MUX switches from phase PH0 to phase PH1 and thus the first pulse of OUT signal is extended to the next phase, i.e., phase PH1, producing a phase shift of T/M. After K/M cycles, the MUX next switches from phase PH1 to phase PH2. This repeats every K/M cycles. After K cycles, the MUX goes through all the phases from phase PH0 to phase PH(M-1) and back to phase PH0 producing K cycles in (K+1)*T seconds. This increases the period from T to T+T/K = T*(K+1)/K, and thus divides the

frequency by (K+1)/K. Consequently, the jitter is reduced to T/M because the suppressed cycle is now only T/M.

It is to be understood that while the above example illustrates shifting up the clock by T/M, the scope of the invention also includes shifting down the clock by T/M, i.e., changing the direction of shifting and reducing the period from T to T-T/M every K/M cycles resulting in K cycles in (K-1)*T seconds. This multiplies the frequency by K/(K-1), as shown in FIG. 3B. FIG. 3C shows a noise spectrum diagram for the resulting jitter. As depicted in FIG. 3C, the frequency of noise is related to how often the phase is shifted, that is the value of M. Also, the energy of the noise is related to the jitter.

FIG. 3D is a simplified timing diagram for the circuit of FIG. 2, where M = 4. As shown by OUT signal, after K/4 cycles, at time s1, the MUX switches from PH0 to PH1 and thus the first pulse of OUT signal is extended to the next phase, i.e., phase PH1, producing a phase shift of Δ, wherein Δ=T/4. After K/4 cycles, the MUX next switches from phase PH1 to phase PH2. This repeats every K/4 cycles. After K cycles, the MUX goes through all the phases from phase PH0 to phase PH3 and back to phase PH0 resulting in K cycles in (K+1)T seconds. This increases the period from T to T+T/4 and divides the frequency by (K+1)/K. Consequently, the jitter is reduced to T/4.

In one embodiment, MUX 21 of FIG. 2 may be placed in the feedback loop of the PLL, i.e., between VCO 20 and PD 10, as shown by MUX 31 in FIG. 4. The input of the MUX 31 is driven by a divide-by-K/M circuit 23 to select one out of M inputs of the MUX. In other words, this scheme feeds back the output of the phase shift to PD 10 through the low pass filter 13 and thus smoothes the clock transition when the phase is shifted from phase PH(k) to phase PH(k±1), resulting in low jitter generation at the output of the VCO. In this embodiment, the jitter energy is further reduced by the low pass filter of the PLL.

The above scheme may be enhanced by using various quantizers as illustrated in FIG. 5. The output of the divide-by-Q 43 is quantized by quantizer 44 to drive MUX 31 selector. A truncator may be used as a quantizer, as shown in FIG. 6A. In this scheme, the j MSB bits of the counter are used to drive the MUX 31, wherein $2^j$=M. FIG. 6B is a simplified circuit diagram of the modified PLL using the truncator of FIG. 6A. In one embodiment, the quantizer is used in combination with the modified PLL of FIG. 2, where the MUX is not in the feedback loop of the PLL.

FIG. 7A shows another example of a quantizer used in one embodiment of the present invention. In this example, a random number generator generates a random number to be added to the value of the counter, resulting in shifting the phase in random. In one embodiment, the random number is added to the value of the counter at a specific time. In another embodiment, at random time intervals, one is added to or subtracted from the value of the counter. The addition and subtraction of one at random time intervals should average out as zero.

Alternatively, a combination of the above two approaches is used, that is, at random time

intervals, a random number is added to the value of the counter to shift the phase in random. As shown in FIG. 7B, the above three approaches spread the quantization noise over the frequency spectrum, rather than at one frequency corresponding to K/M. It should be noted that since the average of the random numbers generated is zero, the average shift in phase is one cycle every K cycles. FIG. 7C is a simplified circuit diagram of the modified PLL using the random number generator of FIG. 7A. In one embodiment, the random number generator is used in combination with the modified PLL of FIG. 2, where the MUX is at the output of the VCO.

FIG. 8A depicts yet an exemplary function of the quantizer circuitry 44. Assuming $2^p = Q$, the output of the divide-by-Q circuit 43 is fed to a quantizer. For this example, an integrator with a transfer function of $Z^{-1}/(1-Z^{-1})$ is used, however, other types of noise shaping blocks may also be used.

Then, p-j output of the integrator is feedback and is subtracted by the k-bit output of the divide-by-Q circuit 43, while j MSB bits of the filter output are truncated and used to control the MUX 31 in FIG. 8C. This is an example of noise shaping using the well-known Sigma-Delta technique. In a Sigma-Delta technique, noise is shifted in frequency domain. As shown in FIG. 8B, the quantization noise is shifted in frequency domain. Although, the noise power may be amplified in this technique, the noise power is shifted to the higher frequency which is reduced significantly by the low pass loop filter 13 of the PLL. FIG. 8C is a simplified circuit diagram of the modified PLL using the integrator of FIG. 8A. In one embodiment, the noise shaping block is used in combination with the modified PLL of FIG. 2, where the MUX is at the output of the VCO.

It will be recognized by those skilled in the art that various modifications may be made to the illustrated and other embodiments of the invention described above, without departing from the broad inventive scope thereof. It will be understood, therefore, that the invention is not limited to the particular embodiments or arrangements disclosed, but is rather intended to cover any changes, adaptations or modifications which are within the scope and spirit of the invention as a system for and a method of dividing or multiplying frequency by a non-integer number with minimum jitter generation by one or more of the above described schemes.

WHAT IS CLAIMED IS:

1. An integrated low jitter frequency multiplication/division electronic circuit for multiplying/dividing frequency of a reference signal, the circuit comprising:

a phase-lock loop (PLL) for generating M number of clock phases from the reference signal; and

a signal shifter electrically coupled to the PLL for shifting the reference signal by one phase every K/M cycle, wherein (K+1)/K is a divisor number and K/(K-1) is a multiplier number.

2. The circuit of claim 1, wherein the signal shifter is a multiplexer (MUX).

3. The circuit of claim 2, wherein the MUX is electrically coupled to the output of the PLL.

4. The circuit of claim 2, wherein the MUX is electrically placed in a feedback loop of the PLL.

5. The circuit of claim 4, further comprising a counter electrically coupled to the MUX for driving the input of the MUX.

6. The circuit of claim 5, wherein the counter drives the input of the MUX to extend the period of the reference signal from T to T+T/M for frequency division.

7. The circuit of claim 6, wherein the counter drives the input of the MUX to reduce the period of the reference signal from T to T-T/M for frequency multiplication.

8. The circuit of claim 4, further comprising a quantizer electrically coupled to the MUX for driving the input of the MUX.

9. The circuit of claim 8, wherein the quantizer is a truncator.

10. The circuit of claim 9, wherein the truncator outputs j most significant bits of the output of a counter to drive the MUX.

11. The circuit of claim 8, wherein the quantizer is a random number added to the output of a counter to drive the MUX.

12. The circuit of claim 8, wherein the quantizer is a noise shaping block electrically coupled to the output of a counter for driving the input of the MUX.

13. The circuit of claim 8, wherein the quantizer is a Sigma-delta noise shaping circuit.

14. The circuit of claim 3, further comprising a counter electrically coupled to the MUX for driving the input of the MUX.

15. The circuit of claim 14, wherein the counter drives the input of the MUX to extend the period of the reference signal from T to T+T/M for frequency division.

16. The circuit of claim 14, wherein the counter drives the input of the MUX to reduce the period of the reference signal from T to T-T/M for frequency multiplication.

17. The circuit of claim 3, further comprising a quantizer electrically coupled to the MUX for driving the input of the MUX.

18. The circuit of claim 17, wherein the quantizer is a random number generator for generating a random number to be added to the output of a counter to drive the input of the MUX.

19. The circuit of claim 17, wherein the quantizer is a random number generator for adding one to or subtracting one from the output of a counter at random time intervals to drive the input of the MUX.

20. The circuit of claim 17, wherein the quantizer is a random number generator for generating a random number and adding the random number at random time intervals to the output of a counter to drive the input of the MUX.

21. The circuit of claim 17, wherein the quantizer is a noise shaping block electrically coupled to the output of a counter to drive the MUX.

22. The circuit of claim 21, wherein the noise shaping block has a transfer function of $Z^{-1}/(1-Z^{-1})$.

23. The circuit of claim 17, wherein the quantizer is a Sigma-delta noise shaping circuit.

24. A method for multiplying/dividing frequency of a reference signal comprising the steps of:

generating M number of clock phases from the reference signal; and

shifting the reference signal by one phase every K/M cycle, wherein (K+1)/K is a divisor number and K/(K-1) is a multiplier number.

25. The method of claim 24, wherein the shifting step comprises extending the period of the reference signal from T to T+T/M for frequency division.

26. The method of claim 24, wherein the shifting step comprises reducing the period of the reference signal from T to T-T/M for frequency multiplication.

27. The method of claim 24, wherein the shifting step comprises using a quantizer electrically coupled to a multiplexer (MUX) for quantizing and driving the input of the MUX.

28. The method of claim 27, wherein the quantizing step comprises of truncating one or more bits of a signal.

29. The method of claim 28, wherein the truncating step comprises of truncating p least significant bits and outputting j most significant bits of the output of a counter to drive the input of the MUX.

30. The method of claim 27, wherein the quantizing step comprises of generating a random number and adding the random number at predetermined time intervals to the output of a counter to drive the input of the MUX.

31. The method of claim 27. wherein the quantizing step comprises of at random time intervals adding one to or subtracting one from the output of a counter to drive the input of the MUX.

32. The method of claim 27, wherein the quantizing step comprises of generating a random number and adding the random number at random time intervals to the output of a counter to drive the input of the MUX.

33. The method of claim 27, wherein the quantizing step comprises electrically coupling to the output of a counter a noise shaping block to drive the input of the MUX.

34. The method of claim 33, wherein the noise shaping block has a transfer function of $Z^{-1}/(1-Z^{-1})$.

35. The circuit of claim 7, wherein the quantizing step comprises using a Sigma-delta noise shaping technique to drive the input of the MUX.

36. A frequency divider for dividing frequency of a reference signal by a non-integer number (K+1)/K comprising:

a clock generator for generating M number of clock phases from the reference signal; and

a signal shifter electrically coupled to the PLL for shifting the reference signal by one phase every K/M cycle.

37. The frequency divider of claim 36, wherein the signal shifter is electrically coupled to the output of the clock generator.

38. The frequency divider of claim 36, wherein the signal shifter is electrically placed in a feedback loop of the clock generator.

39. The frequency divider of claim 36, wherein the clock generator is a phase-lock loop (PLL)

40. The frequency divider of claim 36, wherein the signal shifter is a multiplexer (MUX).

41. The frequency divider of claim 40, further comprising a counter electrically coupled to the MUX for driving the input of the MUX.

42. The frequency divider of claim 40, wherein the counter drives the input of the MUX to extend the period of the reference signal from T to T+T/M.

43. The frequency divider of claim 40, further comprising a quantizer electrically coupled to the MUX for driving the input of the MUX.

44. The frequency divider of claim 43, wherein the quantizer is a noise shaping block.

45. The frequency divider of claim 43, wherein the quantizer is a random number generator for generating a random number and adding the random number at predetermined time intervals to the output of a counter to drive the input of the MUX.

46. The frequency divider of claim 43, wherein the quantizer is a random number generator for adding one to or subtracting one from the output of a counter at random time intervals to drive the input of the MUX.

47. The frequency divider of claim 43, wherein the quantizer is a random number generator for generating a random number and adding the random number at random time intervals to the output of a counter to drive the input of the MUX.

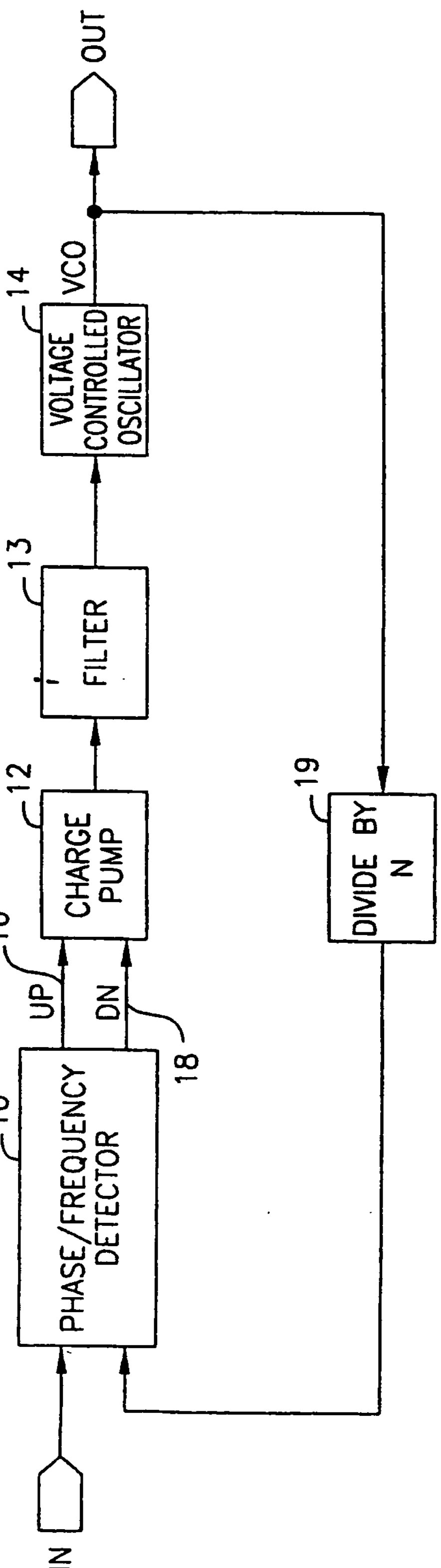



FIG. 1A
PRIOR ART

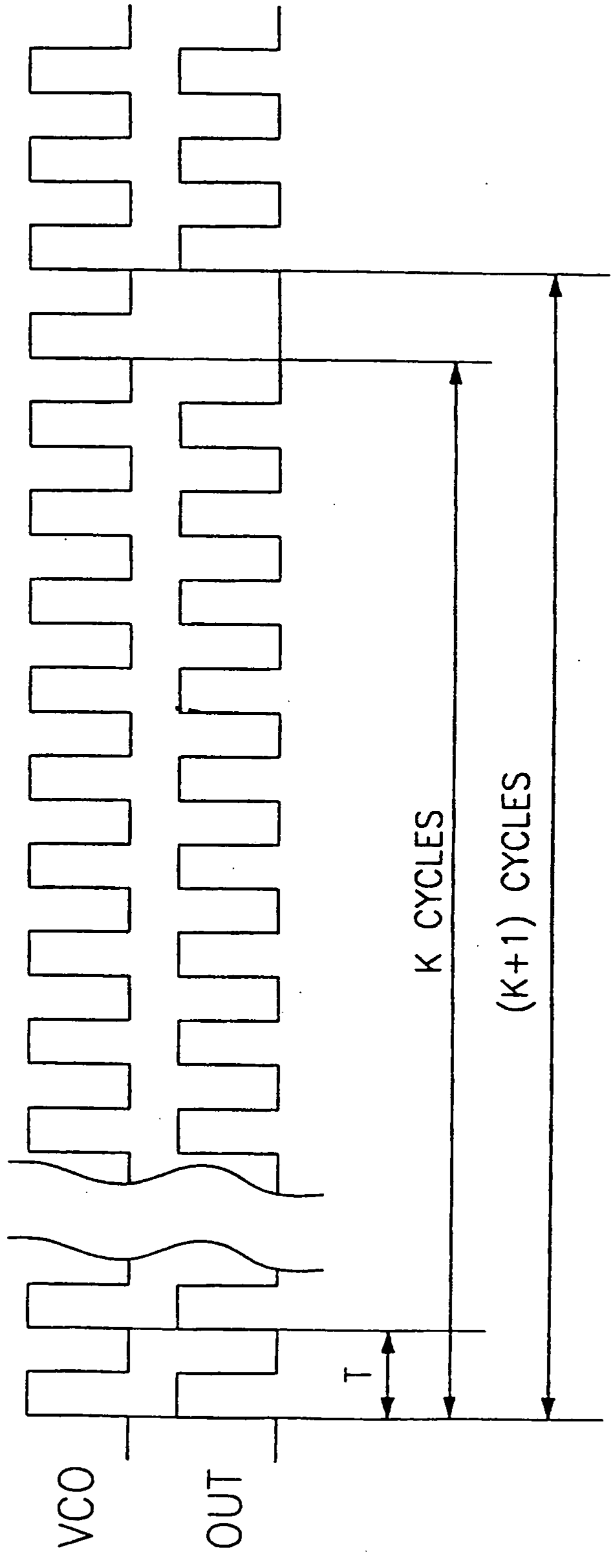
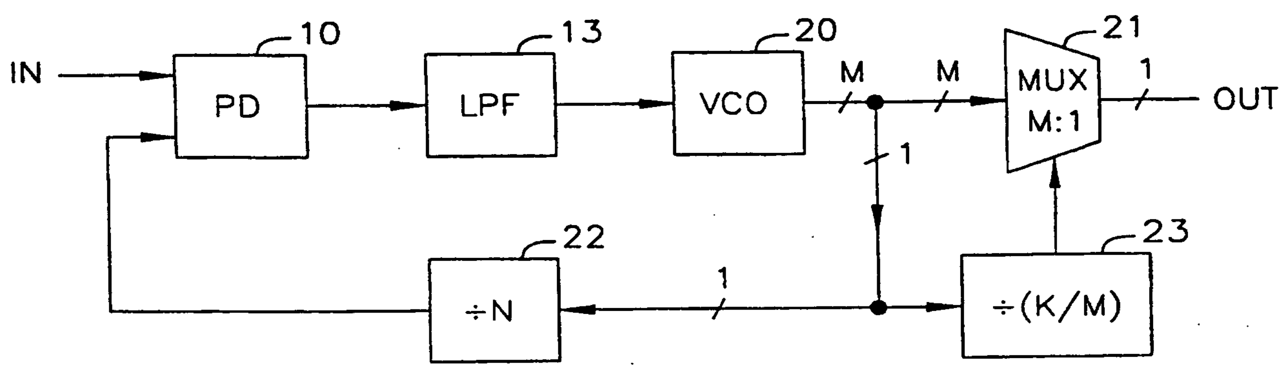



FIG. 1B

*FIG.2*



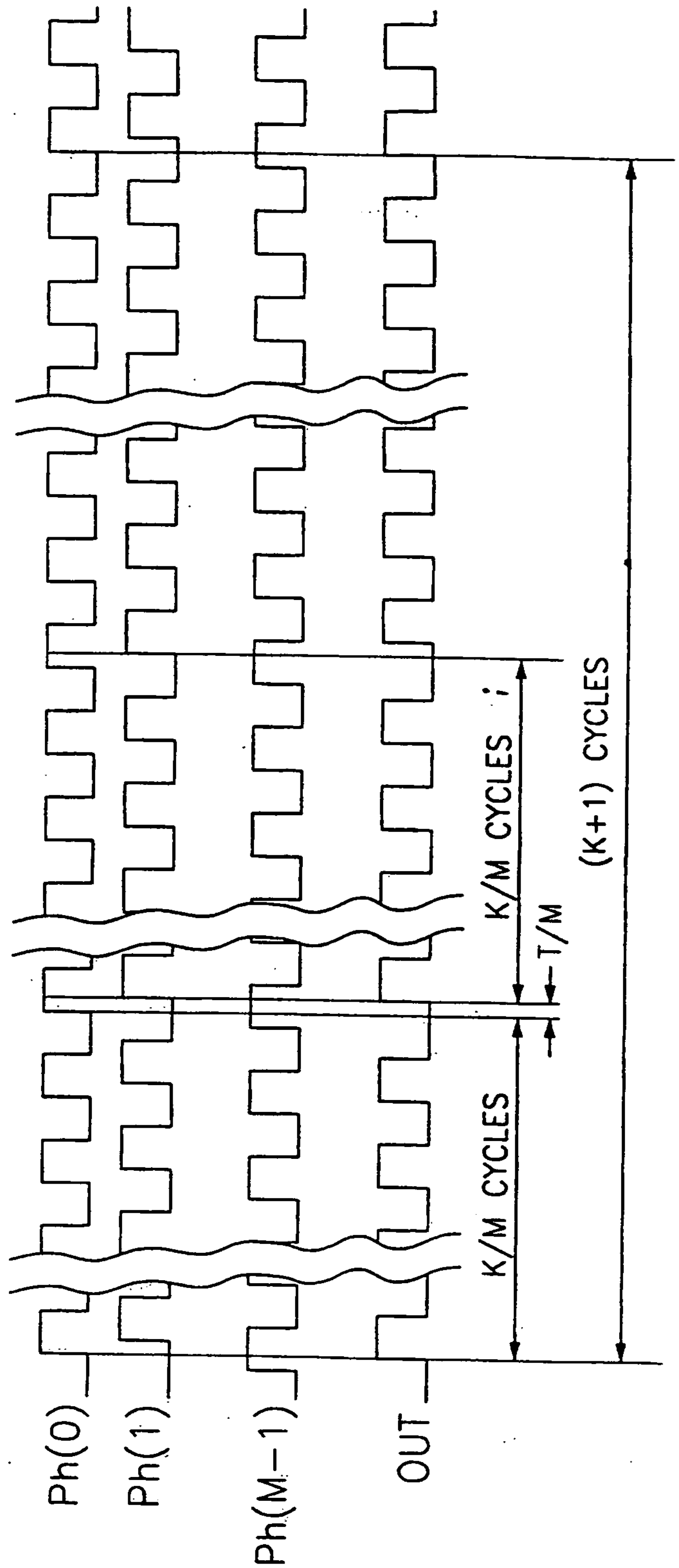



FIG. 3A

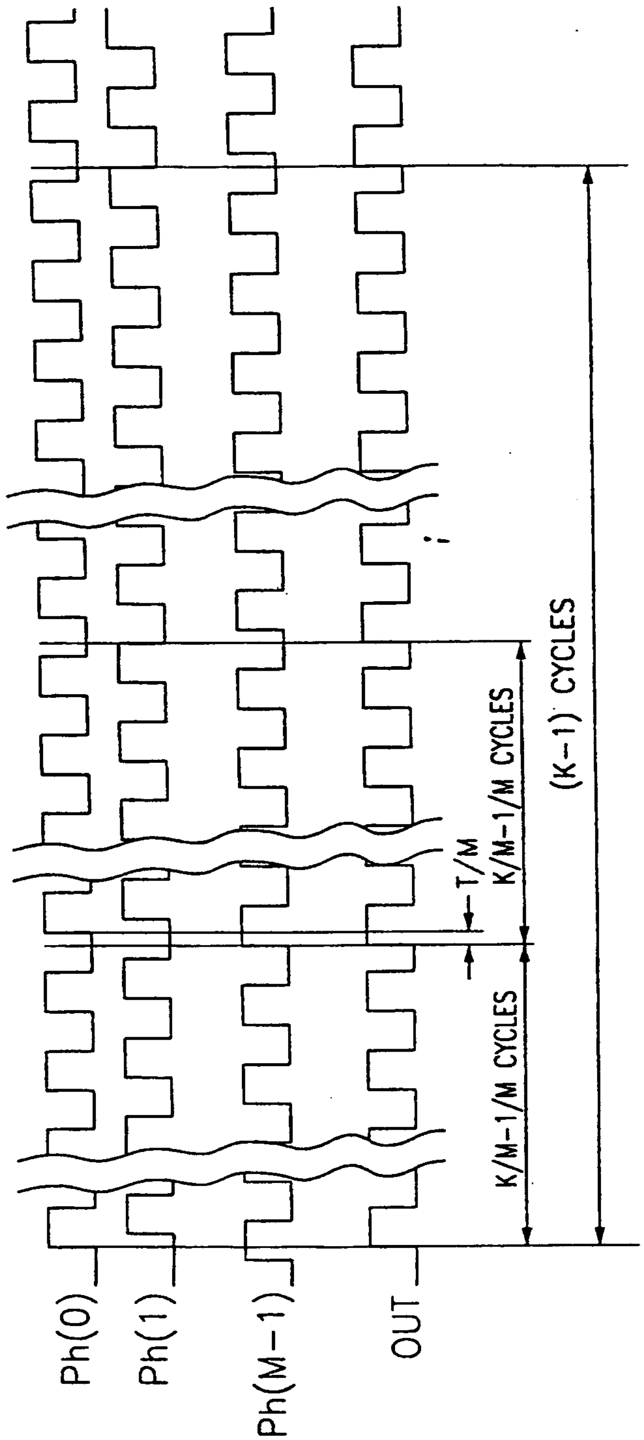



FIG.3B

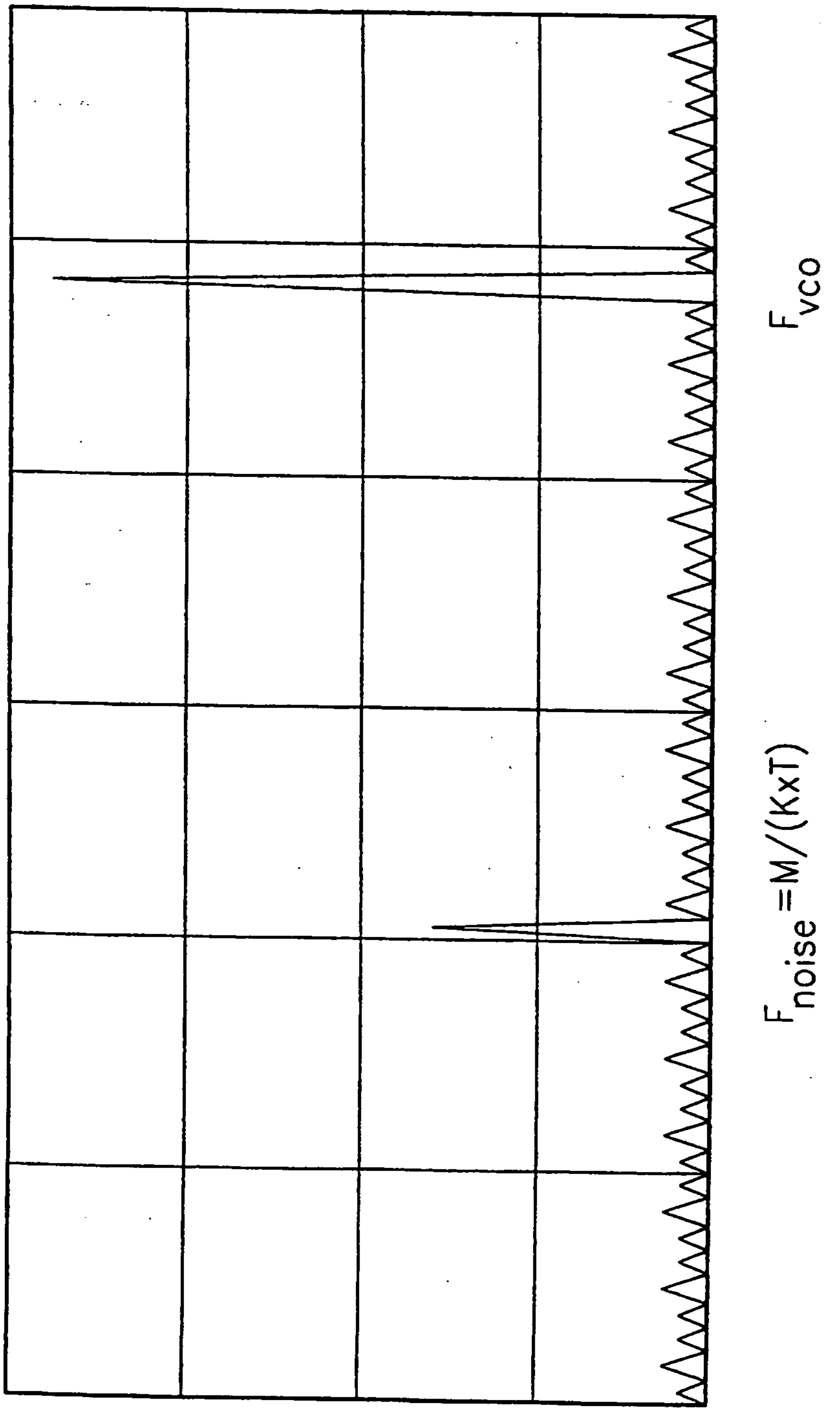



*FIG.3C*

FIG. 3D

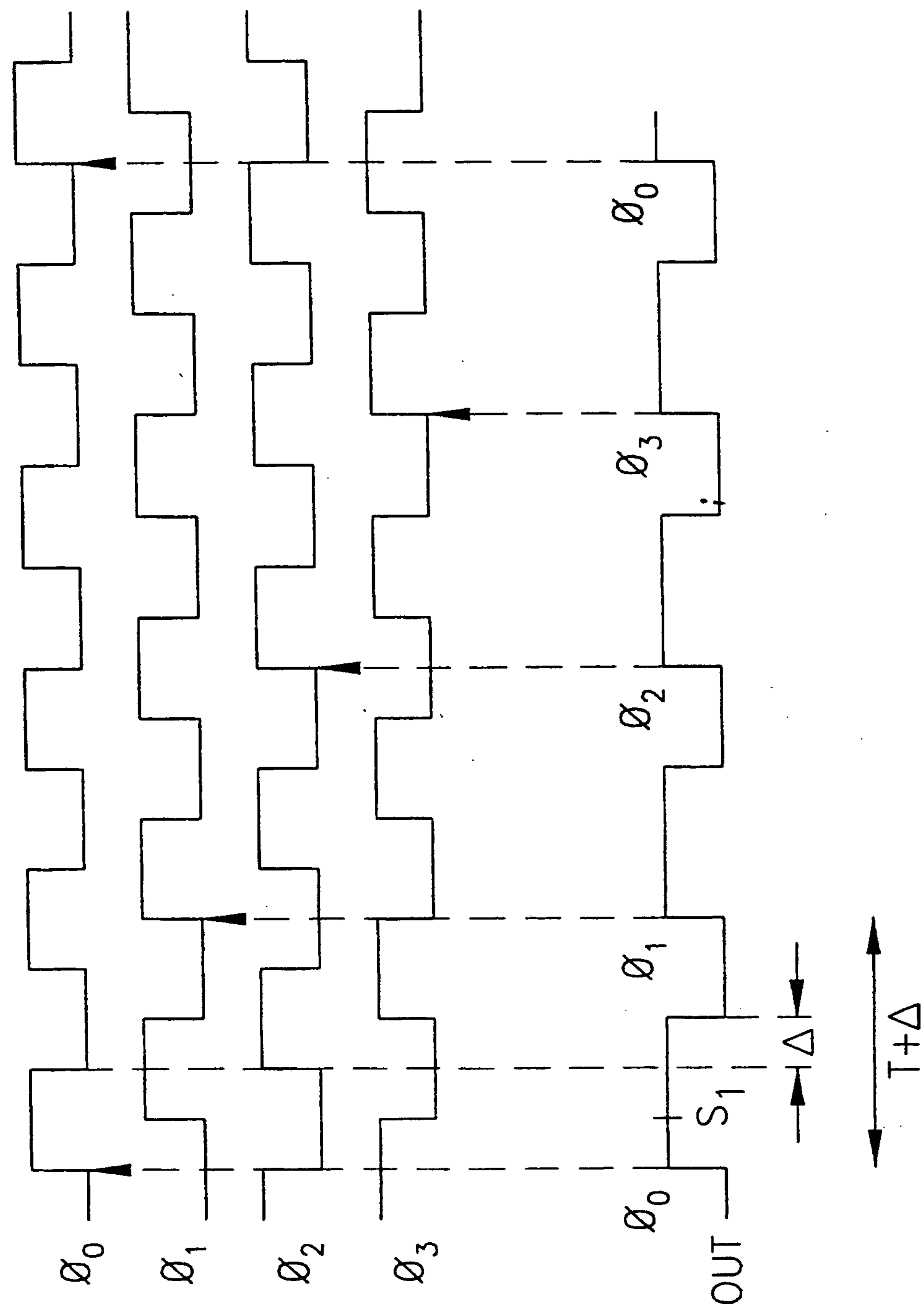


FIG. 4

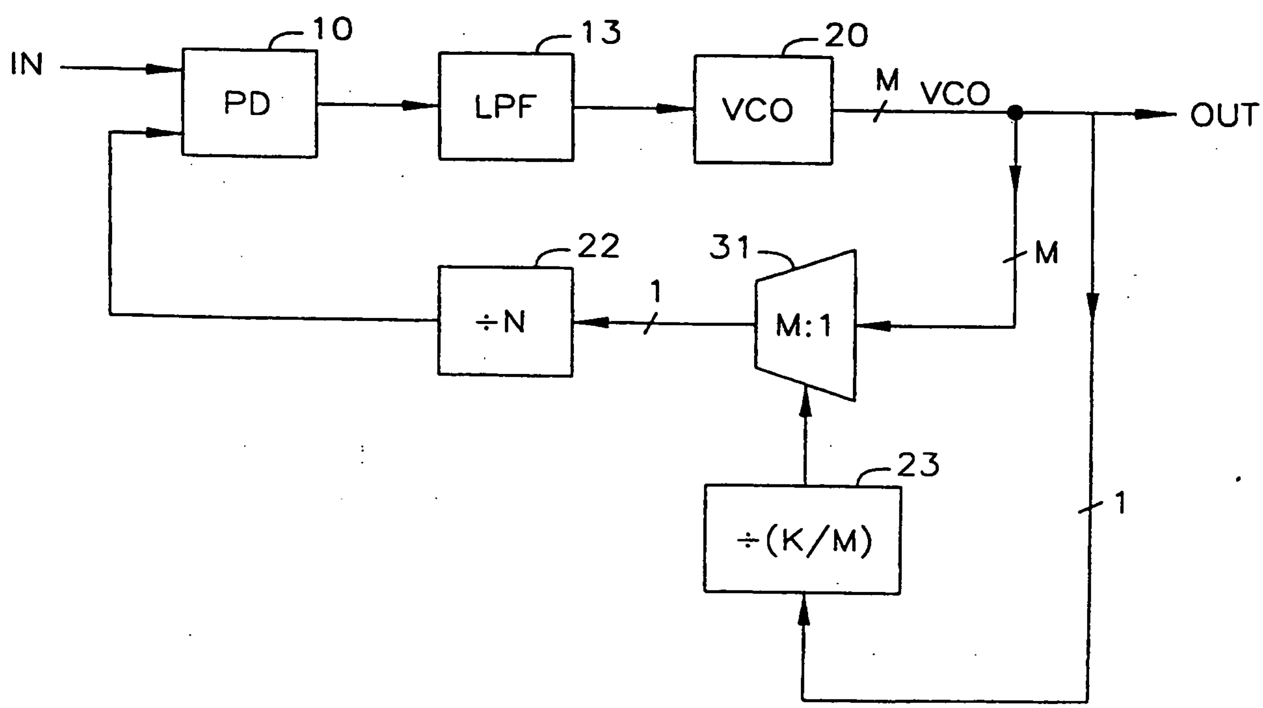


FIG.5

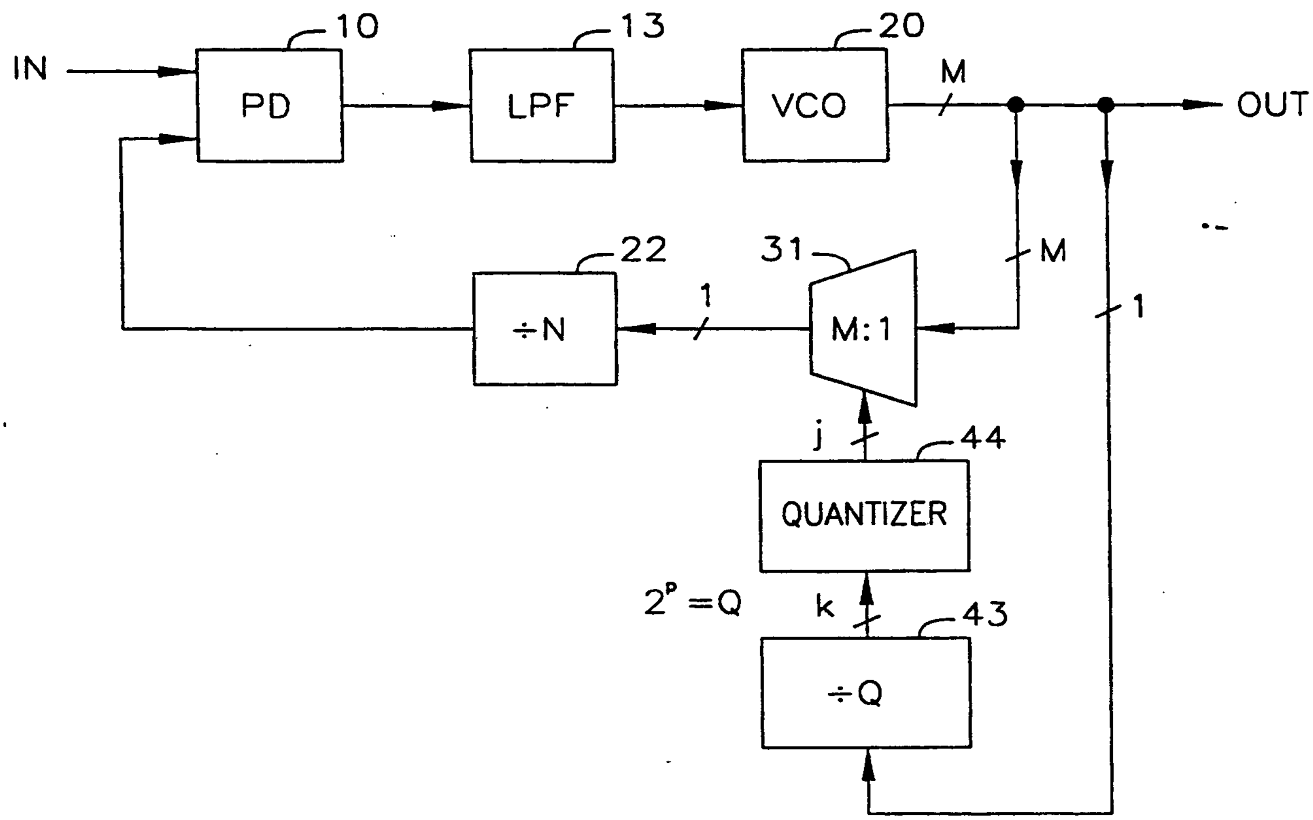
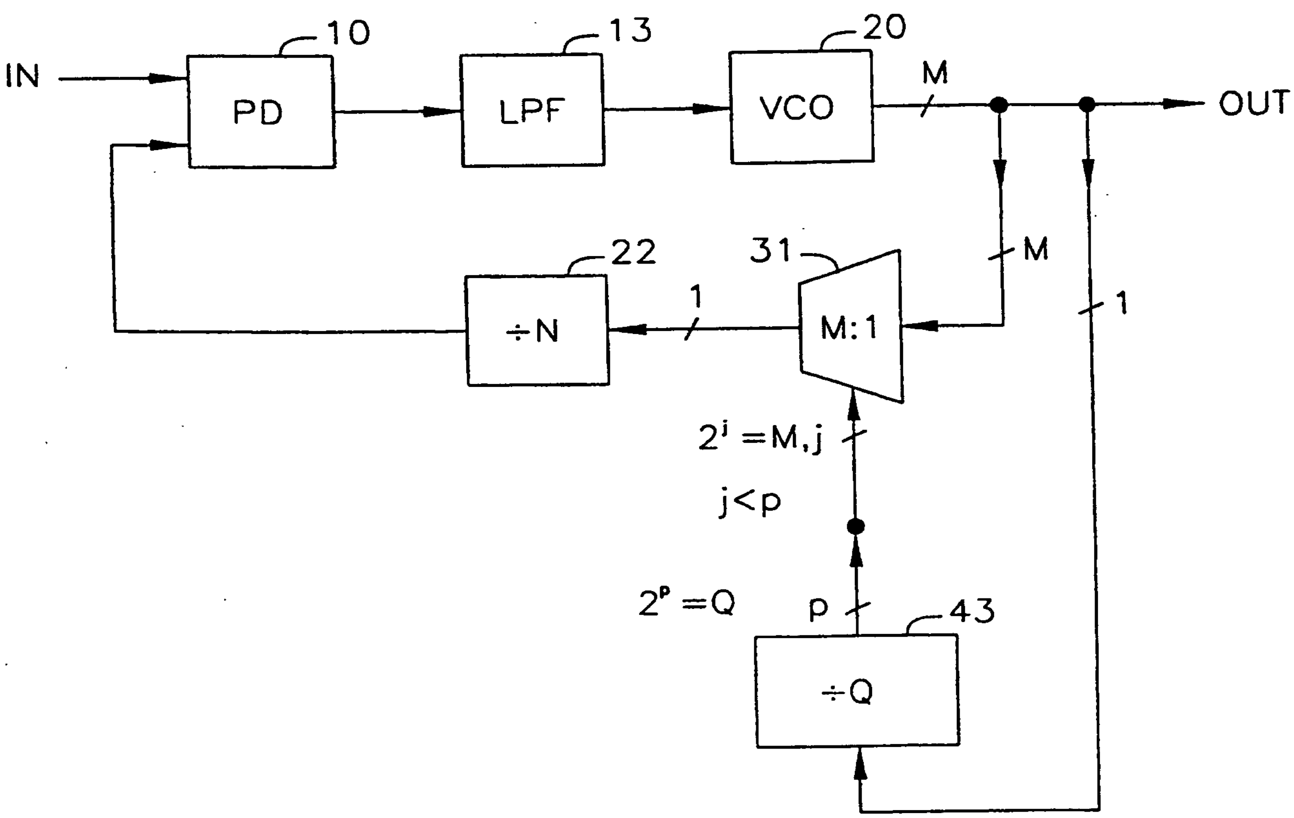
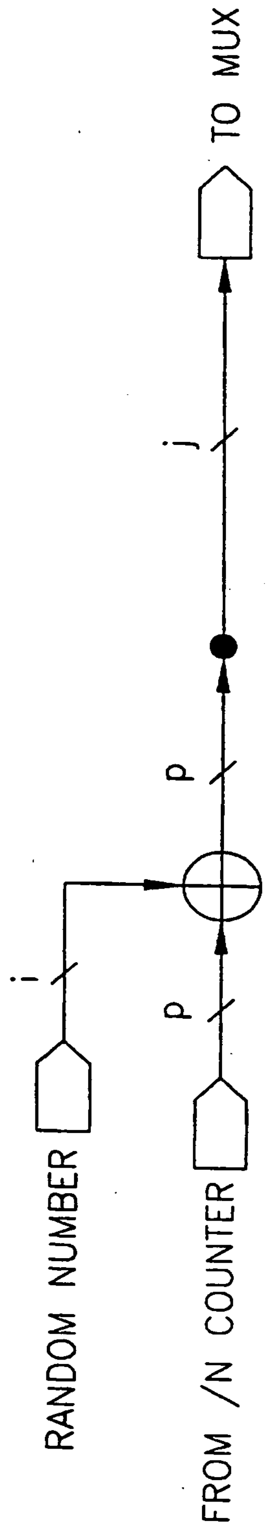



FIG. 6A

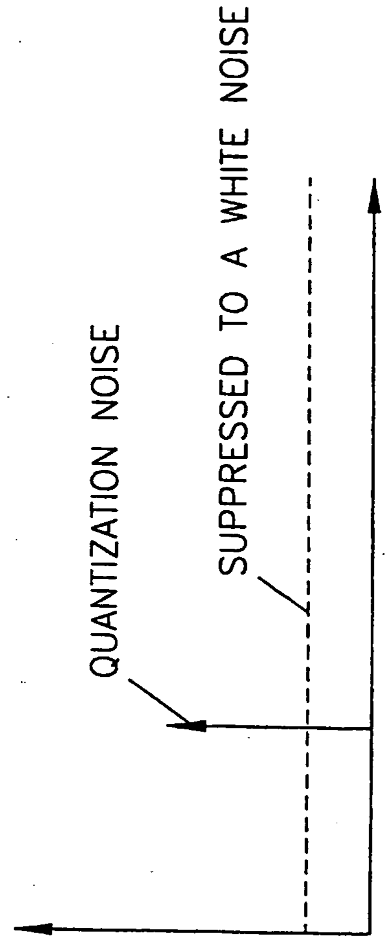
FIG.6B





RANDOM NUMBER
FROM /N COUNTER
i
p
p
j
TO MUX

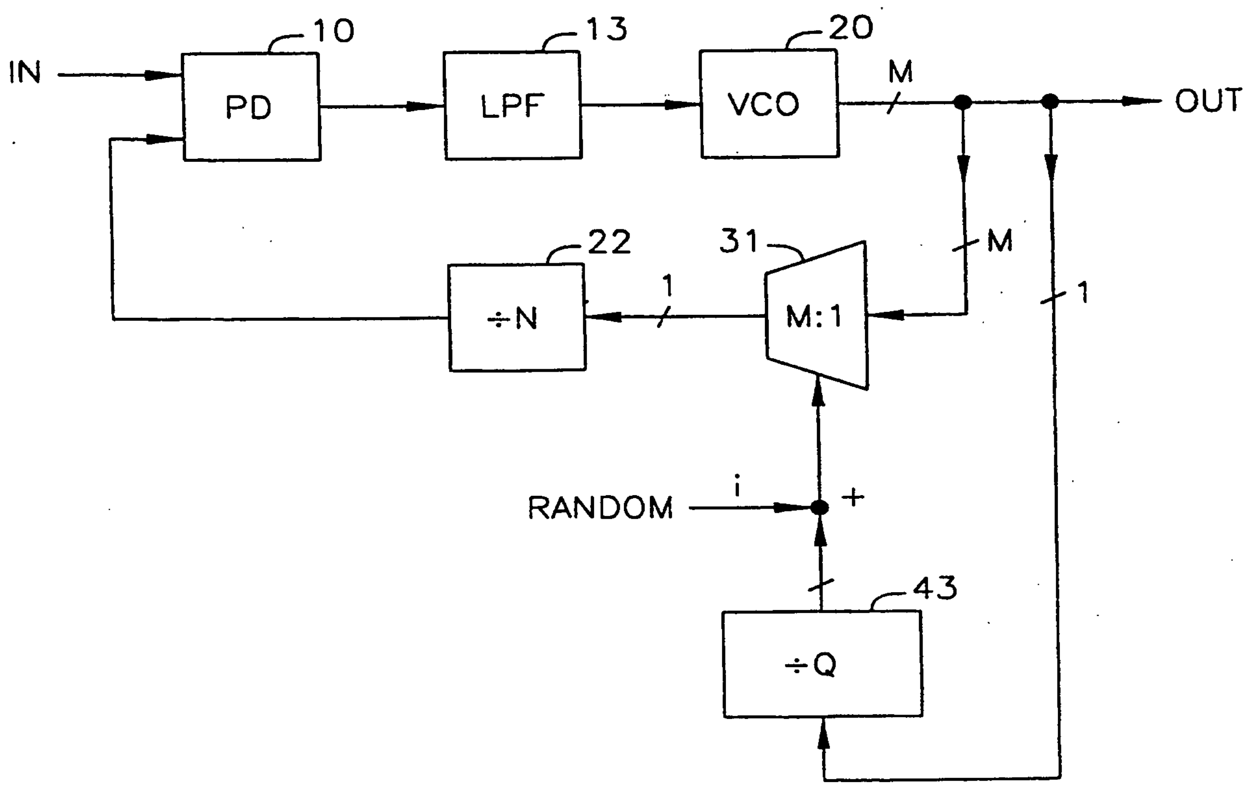

FIG.7A



QUANTIZATION NOISE
SUPPRESSED TO A WHITE NOISE


FIG.7B

*FIG.7C*



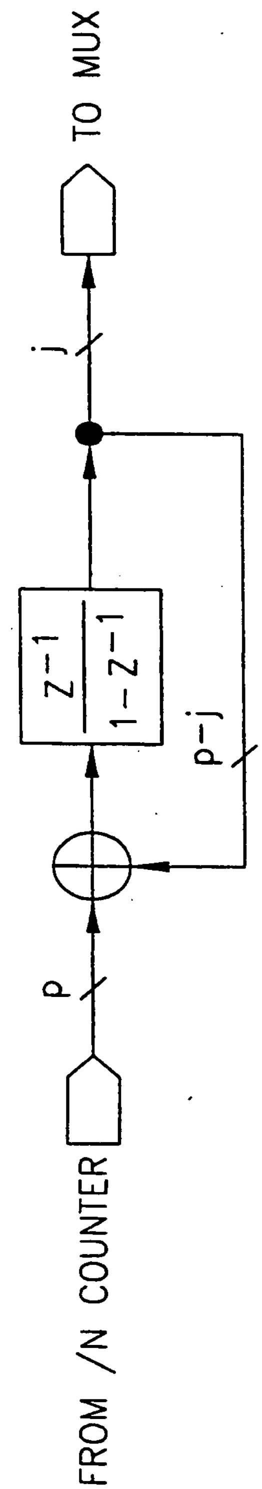

TO MUX
j
$\frac{Z^{-1}}{1-Z^{-1}}$
p−j
p
FROM /N COUNTER

FIG.8A

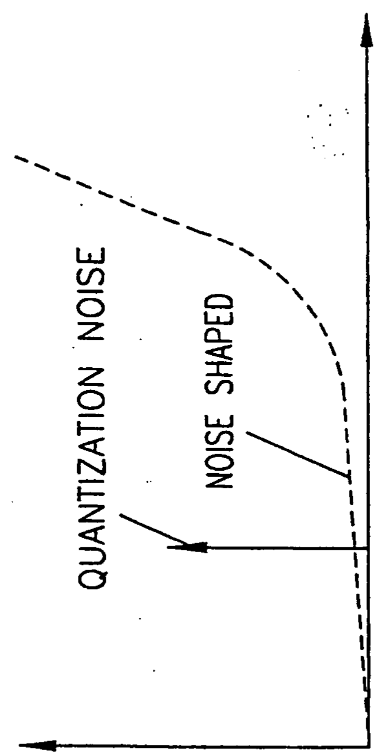
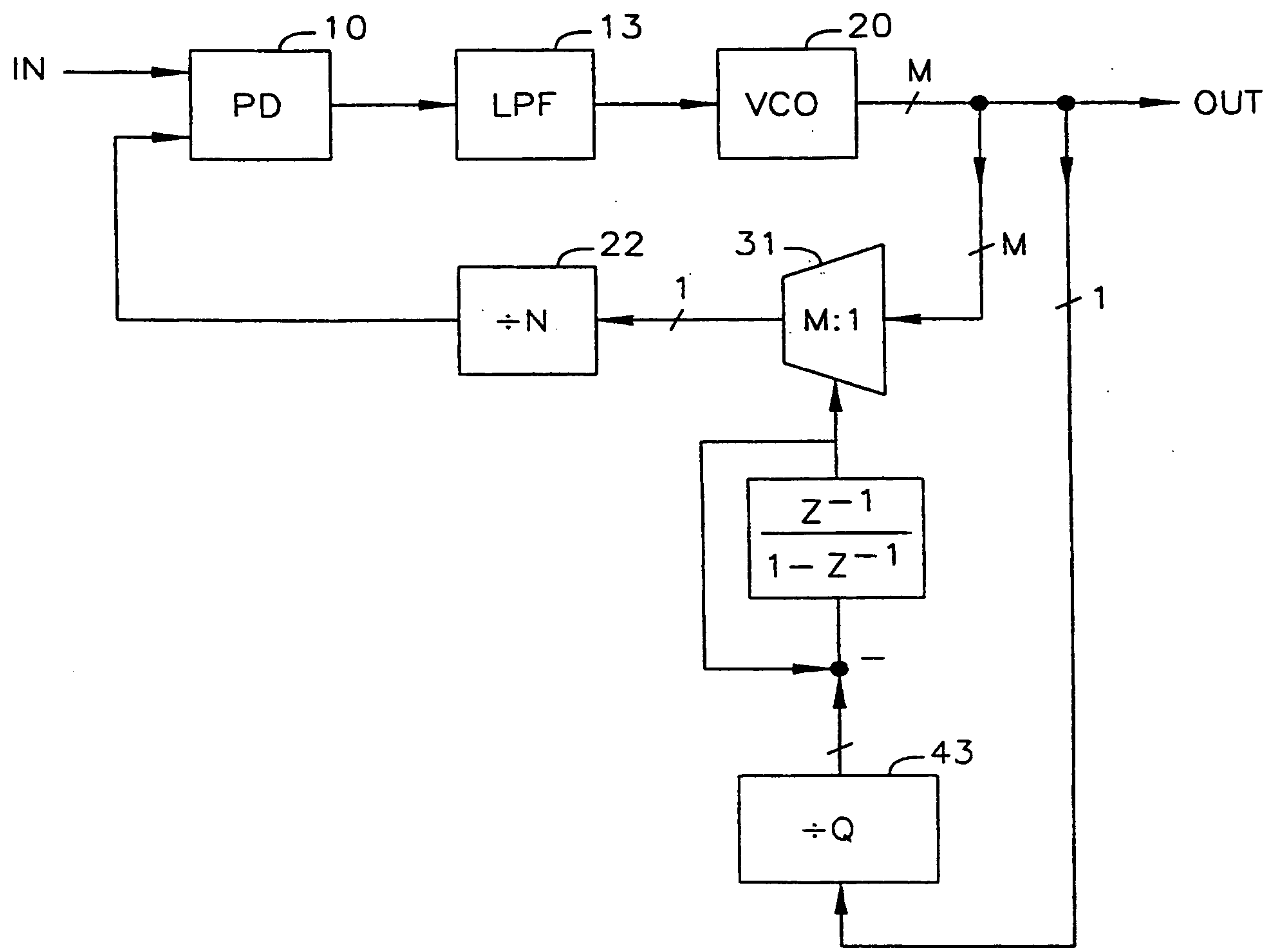

QUANTIZATION NOISE
NOISE SHAPED

FIG.8B

FIG.8C



# INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 00/33908

**A. CLASSIFICATION OF SUBJECT MATTER**
IPC 7 H03L7/081 H03L7/18 H03K5/00 H03K23/68

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03L H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, INSPEC, COMPENDEX, PAJ

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

| Category ° | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X | US 5 889 436 A (WONG KERN WAI ET AL) 30 March 1999 (1999-03-30) column 5, line 53 -column 9, line 8; figures 7-13 --- | 1-7, 14-16, 24-26, 36-42 |
| X | GB 2 325 803 A (LSI LOGIC CORP) 2 December 1998 (1998-12-02) page 4, line 23 -page 7, line 7 page 8, line 12 -page 9, line 4 figures 3,4,6 --- -/-- | 1-3, 14-16, 24-26, 36,37, 39-42 |

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

| Date of the actual completion of the international search | Date of mailing of the international search report |
|---|---|
| 23 April 2001 | 02/05/2001 |

| Name and mailing address of the ISA | Authorized officer |
|---|---|
| European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016 | Balbinot, H |

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

| Category ° | Citation of document, with indication,where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X | WO 90 06017 A (LEVEL ONE COMMUNICATIONS INC) 31 May 1990 (1990-05-31)<br>page 6, line 13 -page 12, line 14; figures<br>--- | 1,2,4-7, 24-26, 36-42 |
| P,X | EP 1 045 518 A (INFINEON TECHNOLOGIES CORP) 18 October 2000 (2000-10-18)<br>column 2, line 6 -column 5, line 10; figures 1-3B<br>----- | 1-4, 24-26, 36-40 |

# INTERNATIONAL SEARCH REPORT

Information on patent family members

Interna al Application No
PCT/US 00/33908

| Patent document cited in search report | Publication date | Patent family member(s) | Publication date |
|---|---|---|---|
| US 5889436 A | 30-03-1999 | NONE | |
| GB 2325803 A | 02-12-1998 | NONE | |
| WO 9006017 A | 31-05-1990 | CA 2002382 A<br>US 5059924 A | 07-05-1990<br>22-10-1991 |
| EP 1045518 A | 18-10-2000 | NONE | |